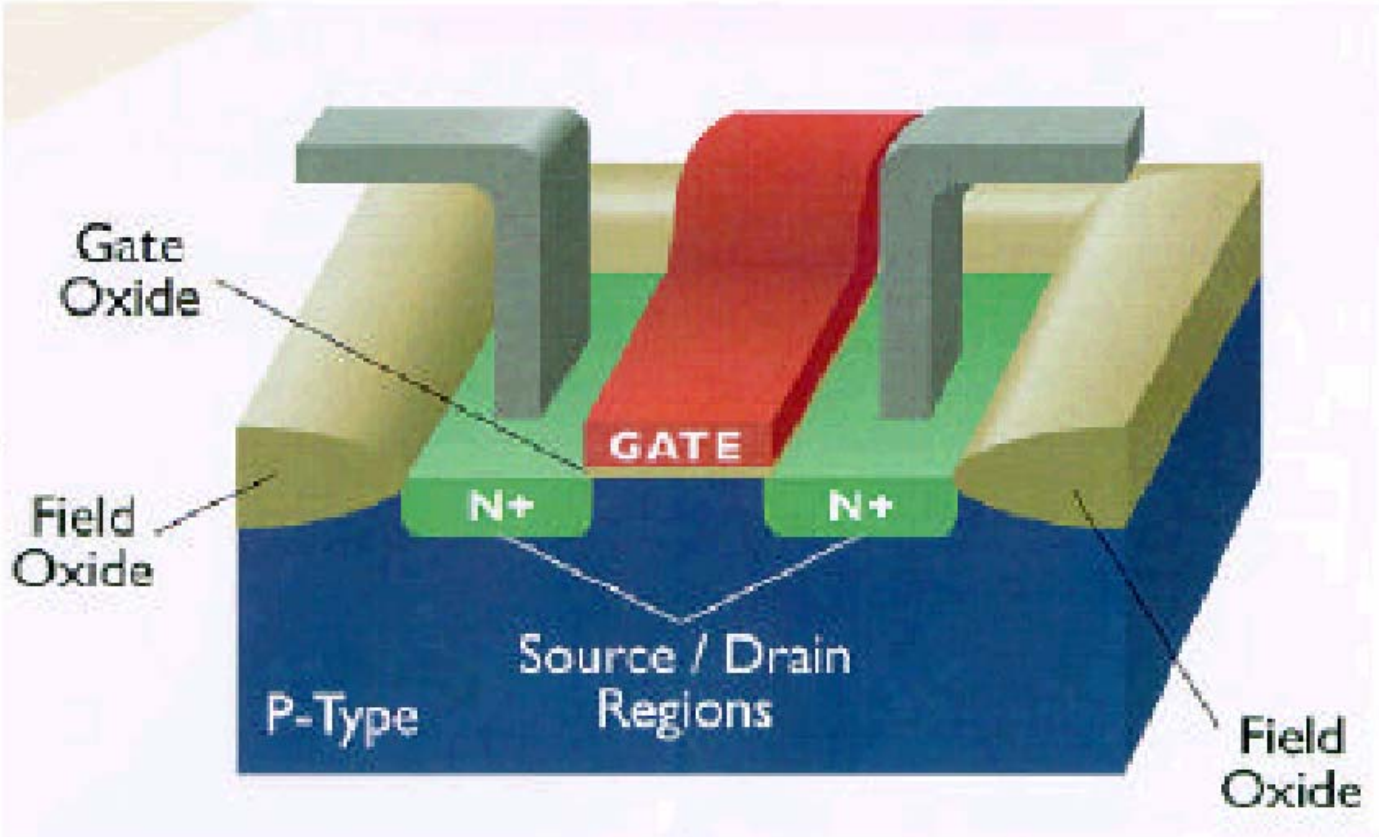
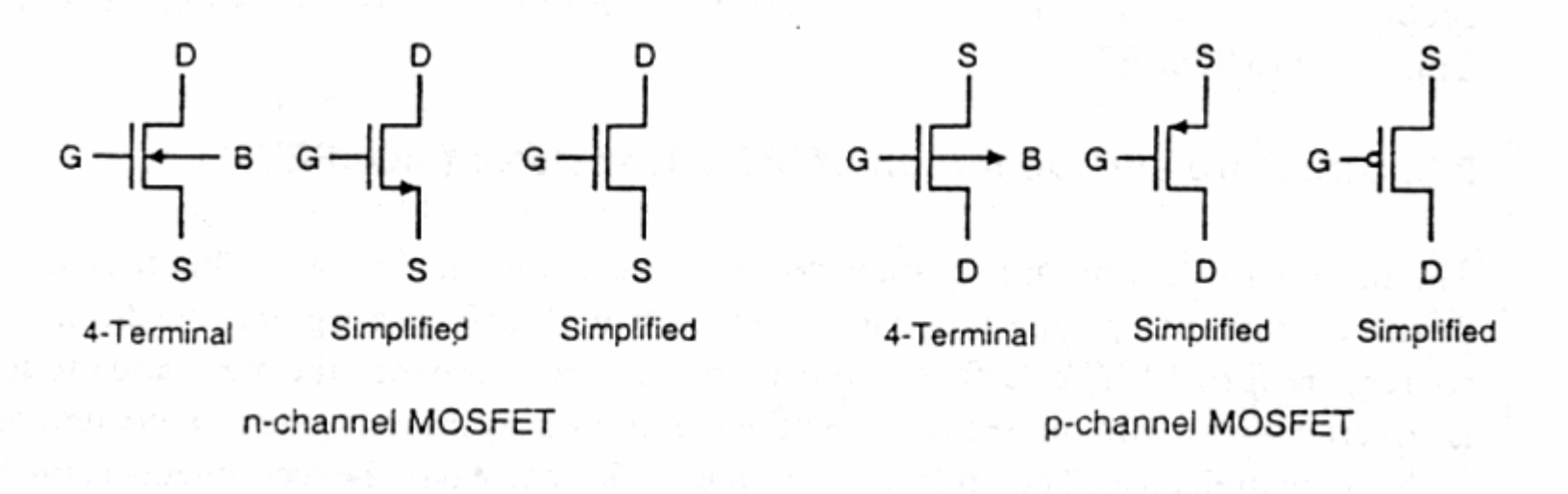
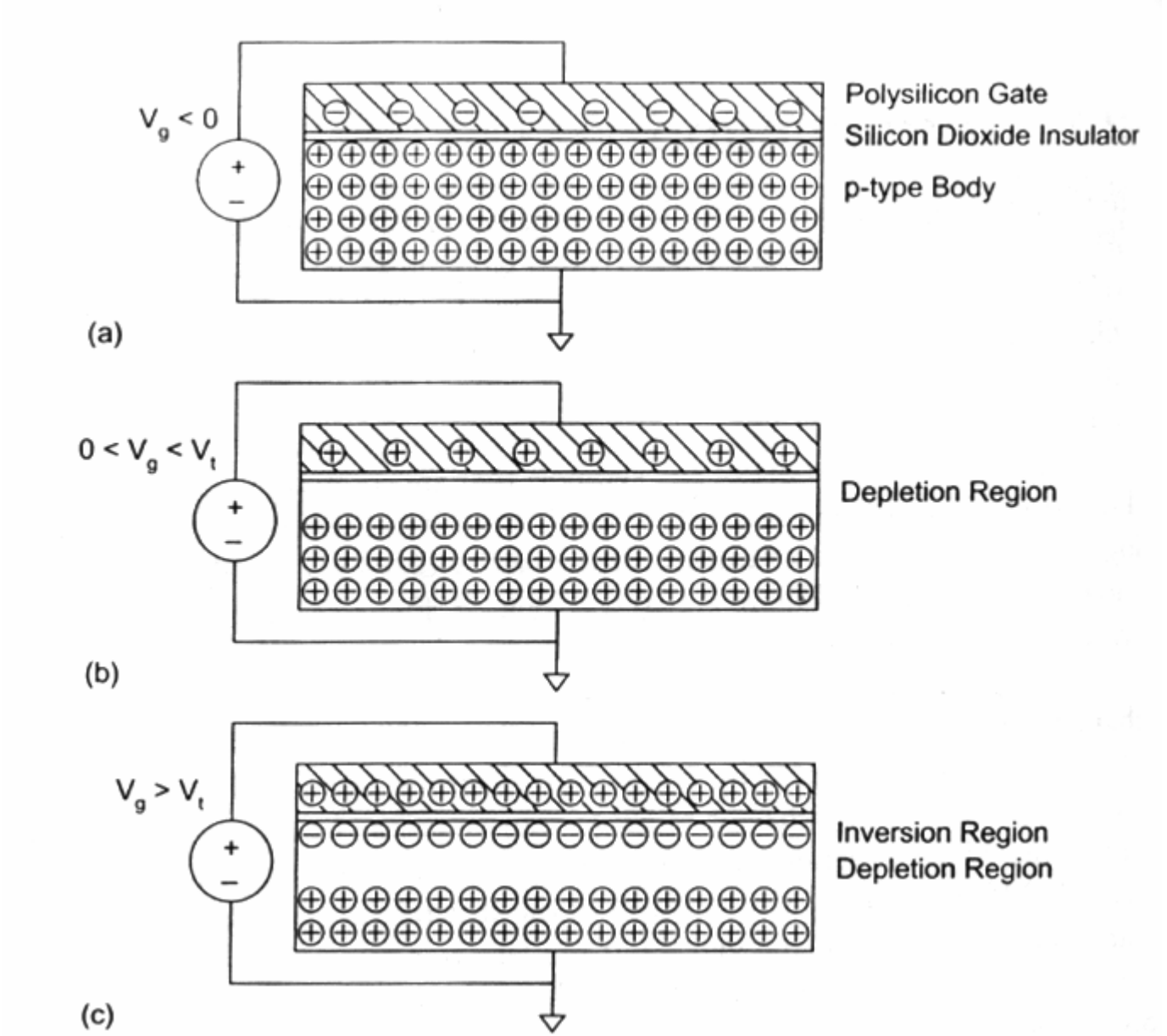
Metal Oxide Semiconductor (MOS) TRANZISTOR N-TIPA



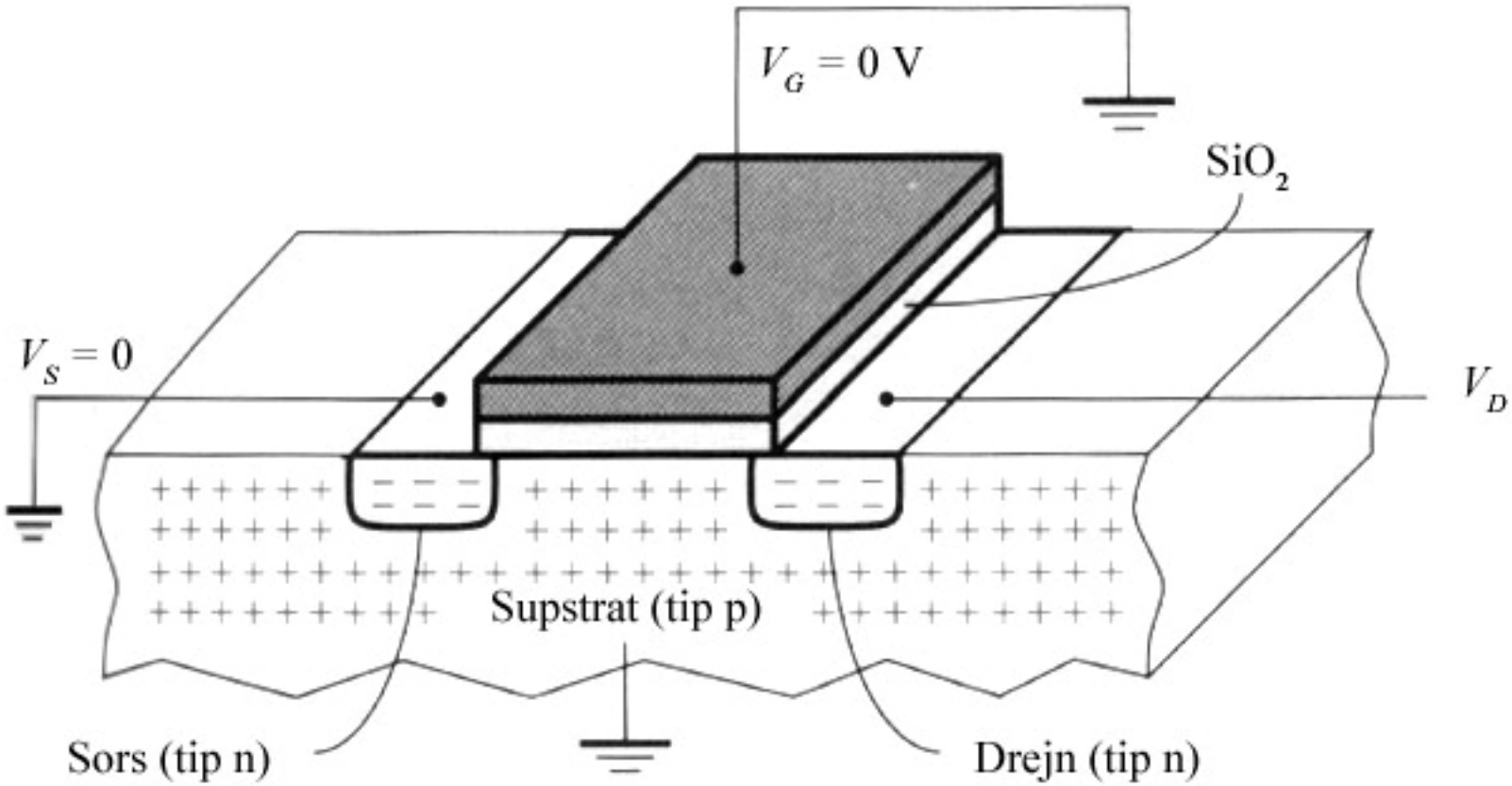
Simboli MOSFET-a



FORMIRANJE KANALA

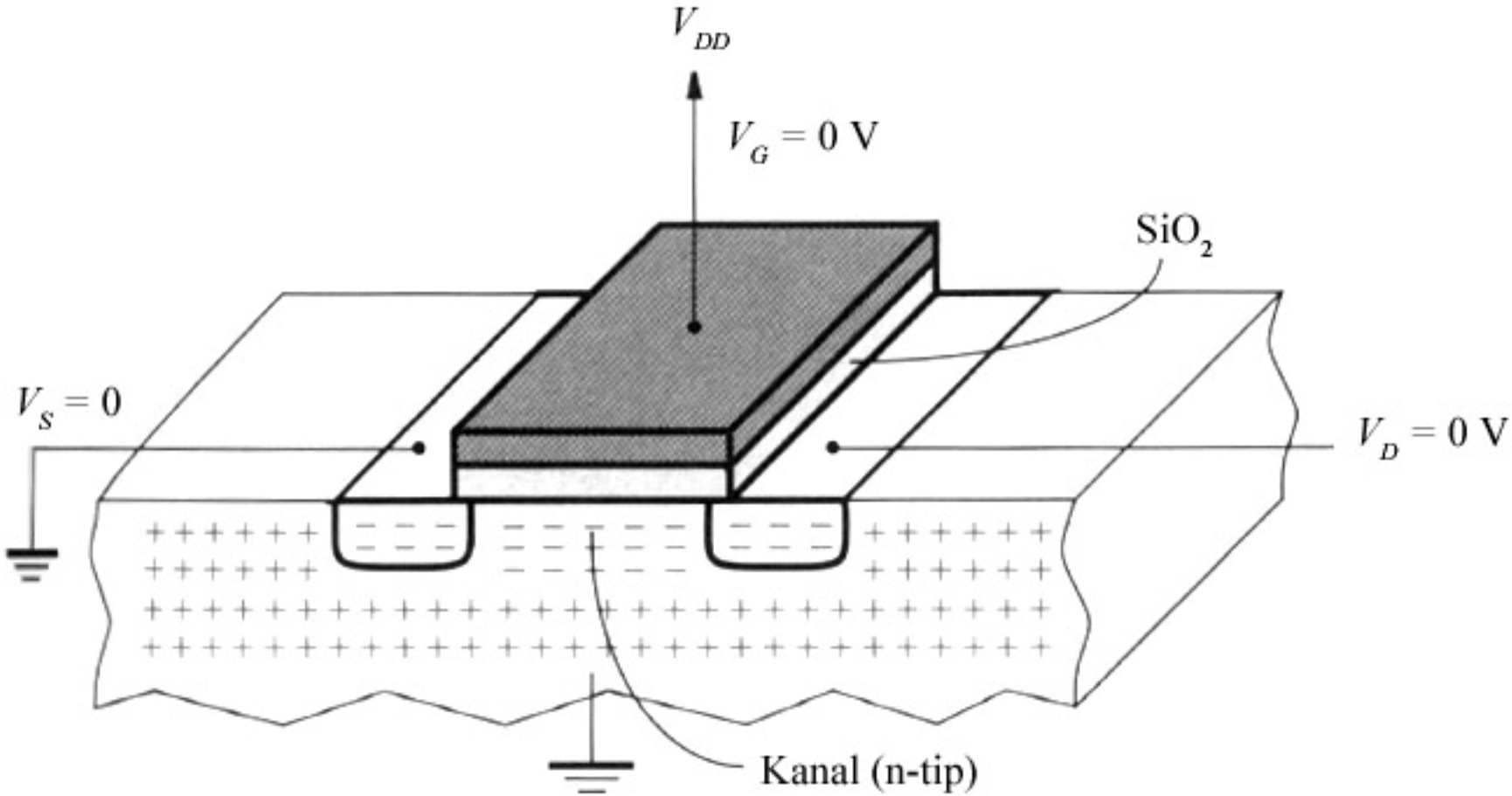


NMOS TRANZISTOR - ISKLJUČEN



(a) Kada je $V_{GS} = 0$ V, tranzistor je isključen

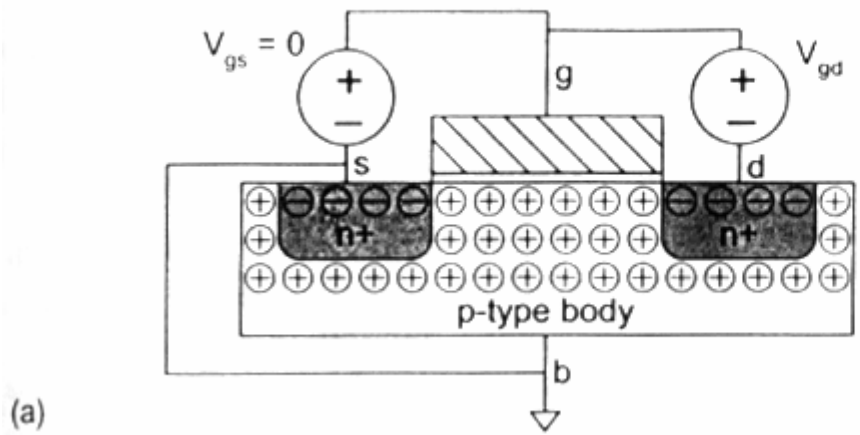
NMOS TRANZISTOR - UKLJUČEN



(b) Kada je $V_{GS} = 5$ V, tranzistor je uključen

NMOS - u stanju zakočenja

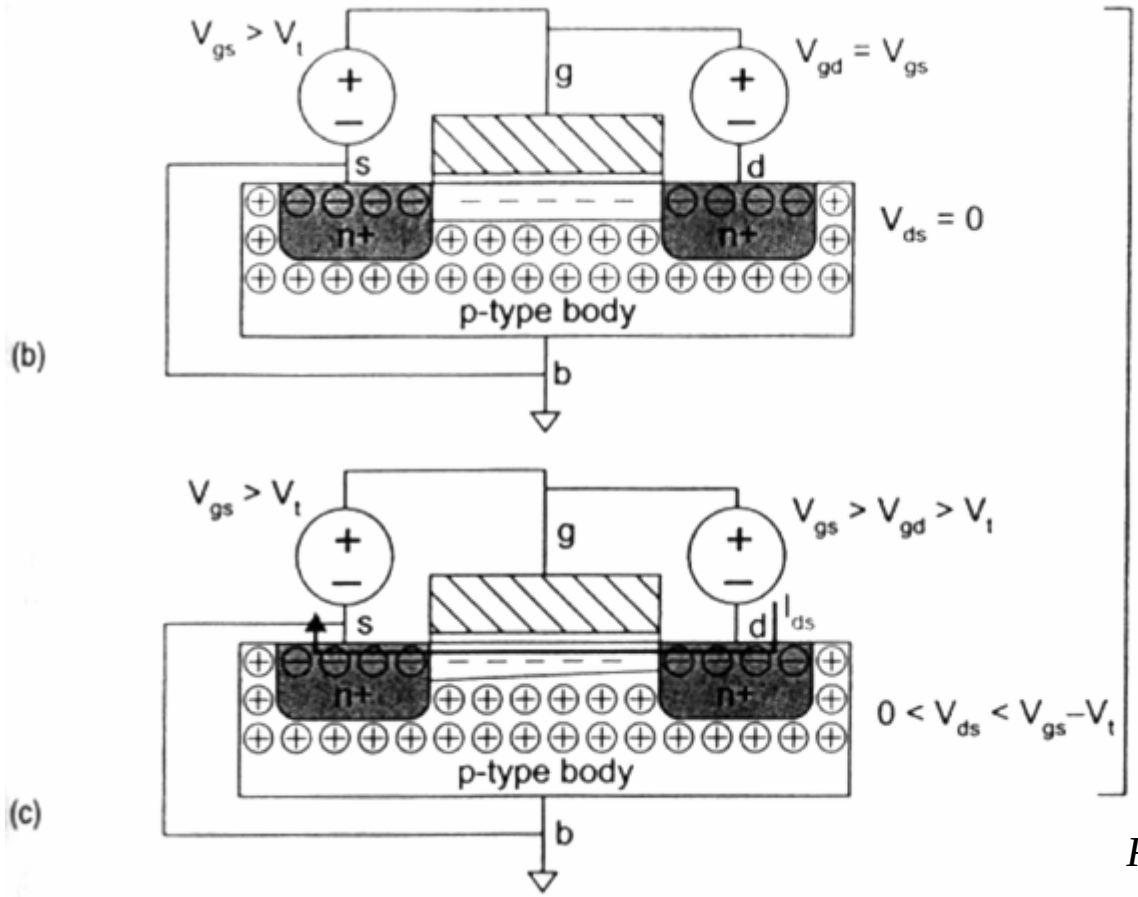
$U_{gs} < V_T$



Cutoff:
No Channel
$I_{ds} = 0$

NMOS - u linearnoj oblasti (omska oblast)

$$I_D = k_n' \frac{W}{L}\left[(U_{GS} - V_T)V_{DS} - \frac{1}{2}U_{DS}^2\right]$$



$U_{gs} > V_T$

$U_{ds} < U_{gs} - V_T$

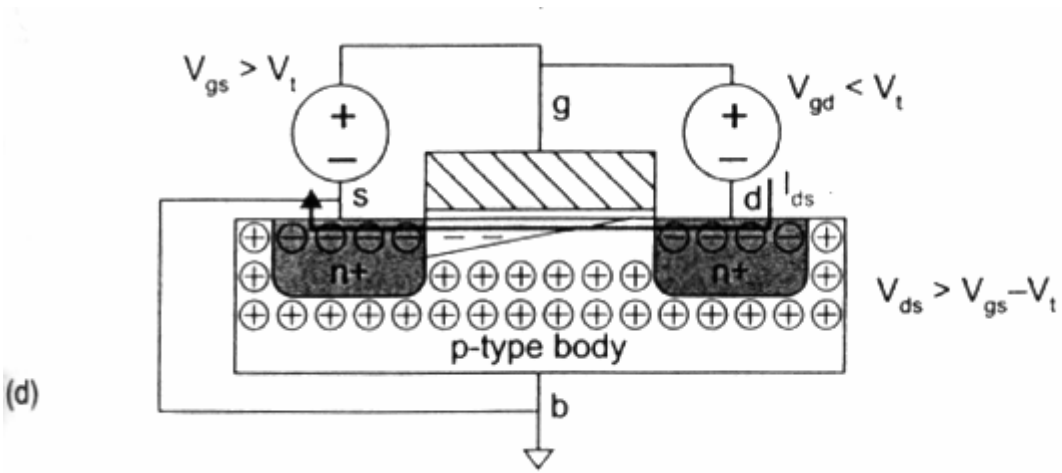
Linear:
Channel Formed
I_{ds} Increases with V_{ds}

$$R_{DS} = U_{DS}/I_D = 1/\left[k_n' \frac{W}{L}(U_{GS} - V_T)\right]$$

NMOS - oblast zasicenja (karakteristika)

$$I_D = \frac{1}{2} k'_n \frac{W}{L} \left(V_{GS} - V_T\right)^2$$

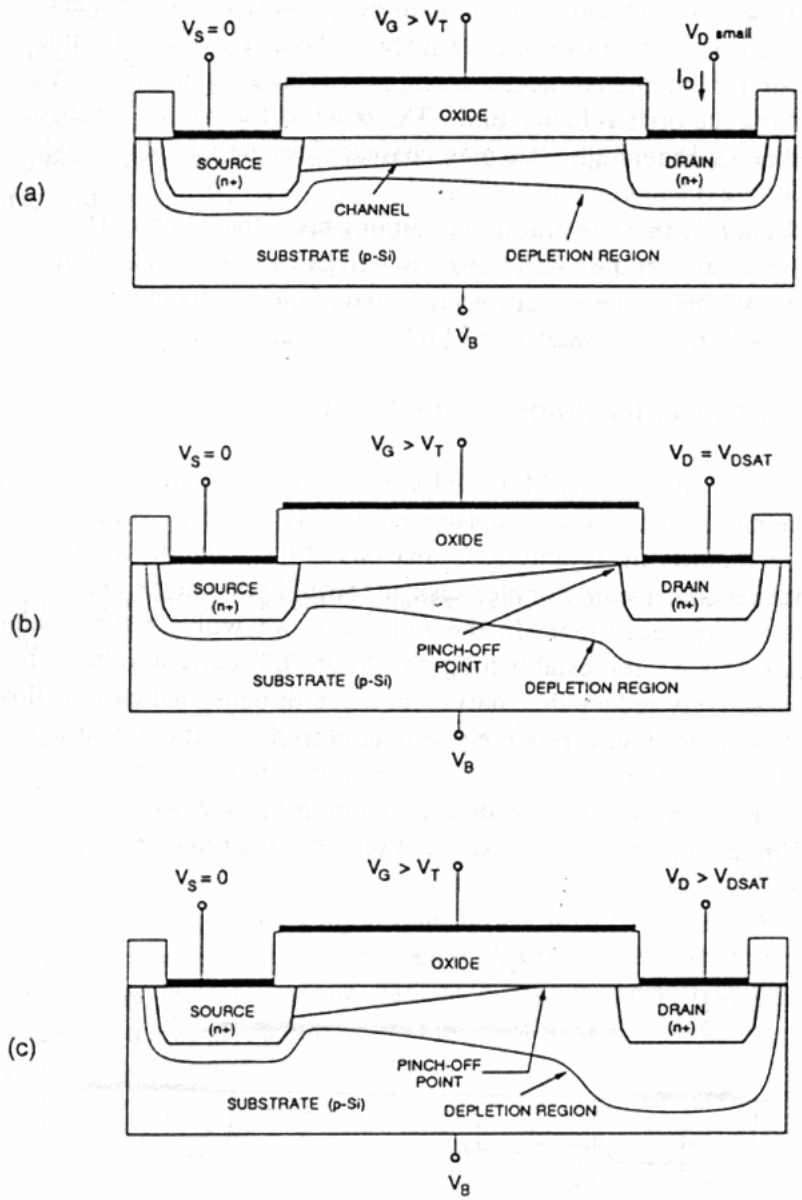
$$k'_N = \left(2 \div 2{,}5\right) \cdot k'_P$$



$U_{gs} > V_T$

$U_{ds} > U_{gs} - V_T$

Saturation:
Channel Pinched Off
I_{ds} Independent of V_{ds}



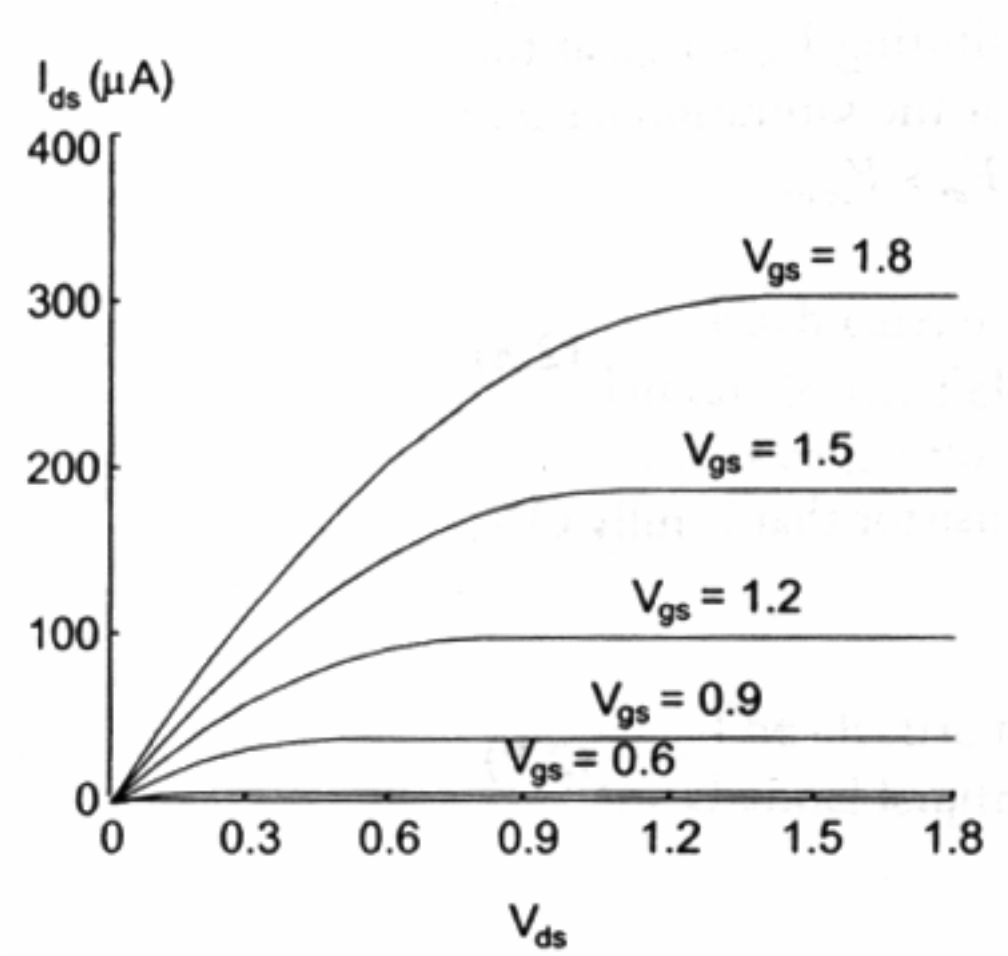
(a) Omska oblast

(b) Granica između omske oblasti i oblasti zasićenja

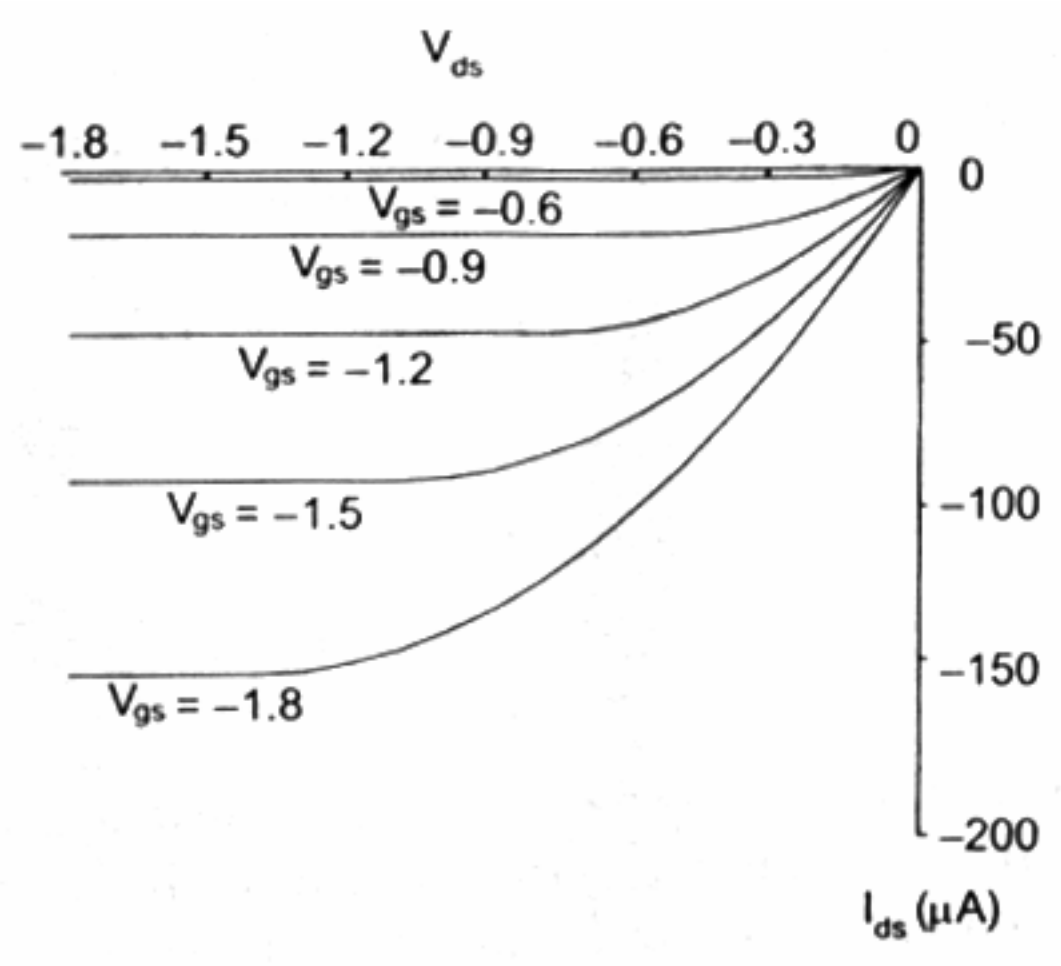
$U_{ds} = U_{gs} - V_T$

(c) Oblast zasićenja karakteristika

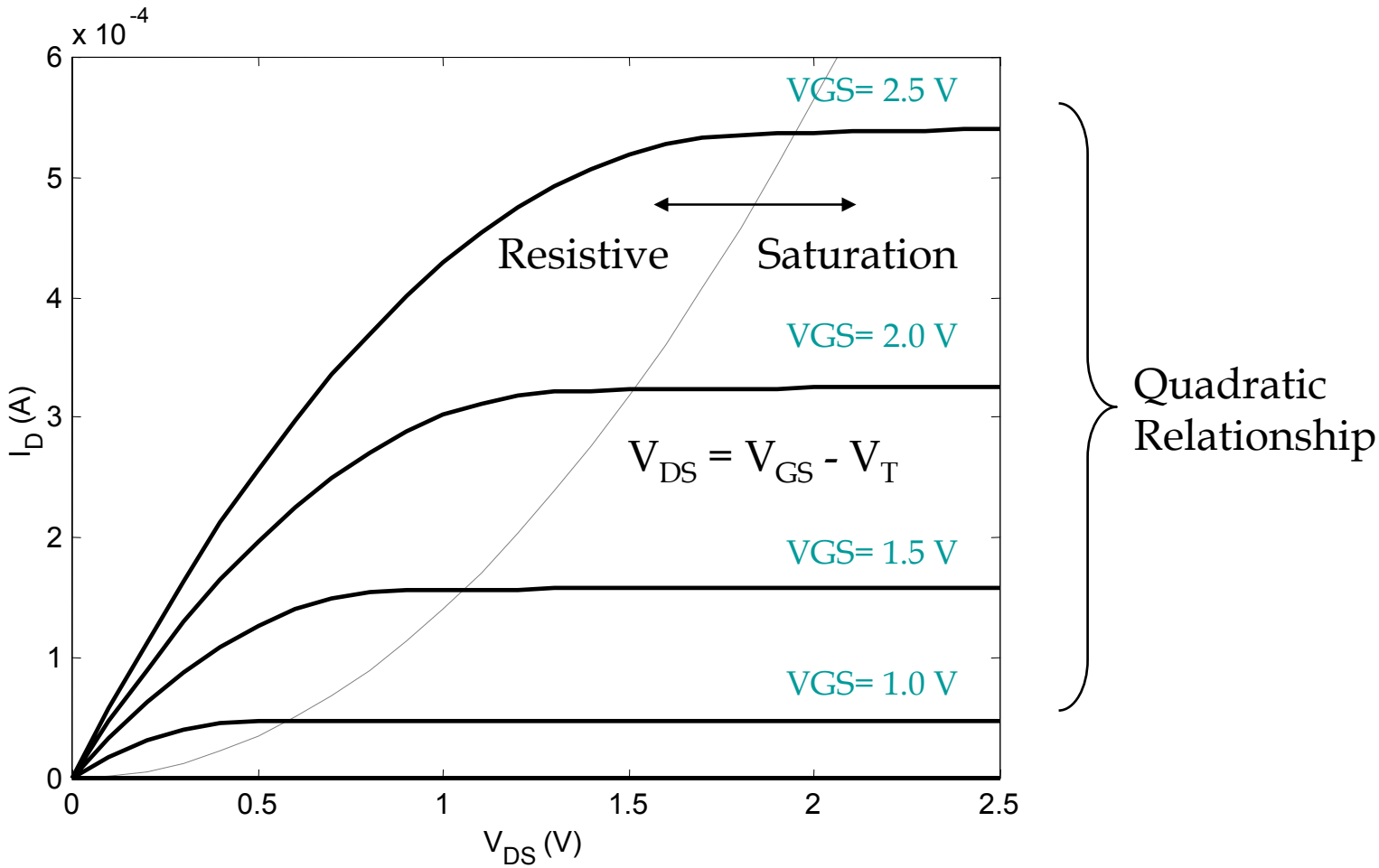
Izlazna karakteristika idealnog NMOS tranzistora



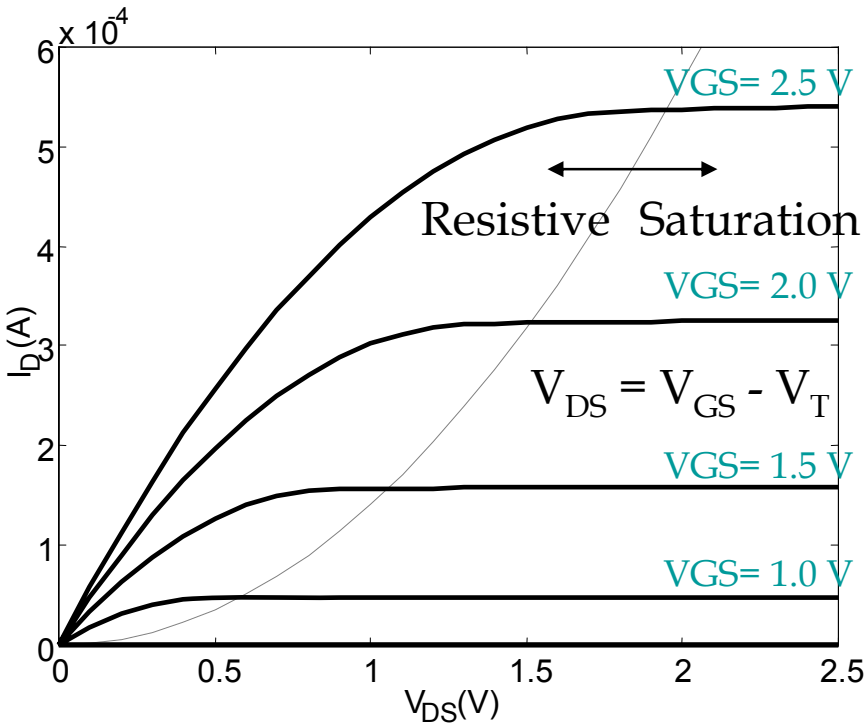
Izlazna karakteristika idealnog PMOS tranzistora



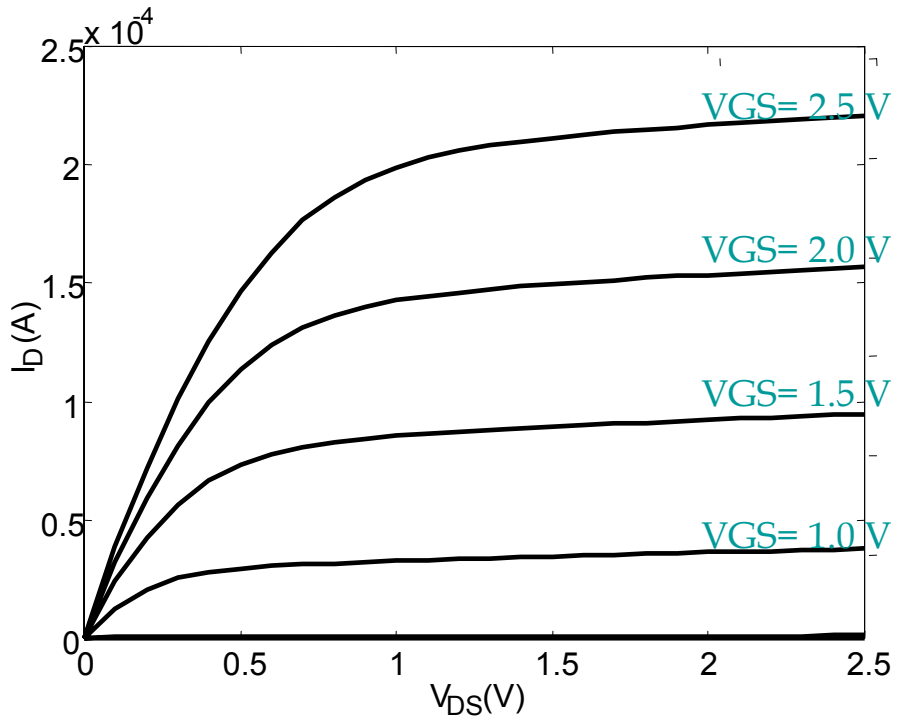
OBLASTI RADA NA STRUJNO-NAPONSKOJ KARAKTERISTICI NMOS TRANZISTORA



STRUJNO-NAPONSKA KARAKTERISTIKA NMOS TRANZISTORA

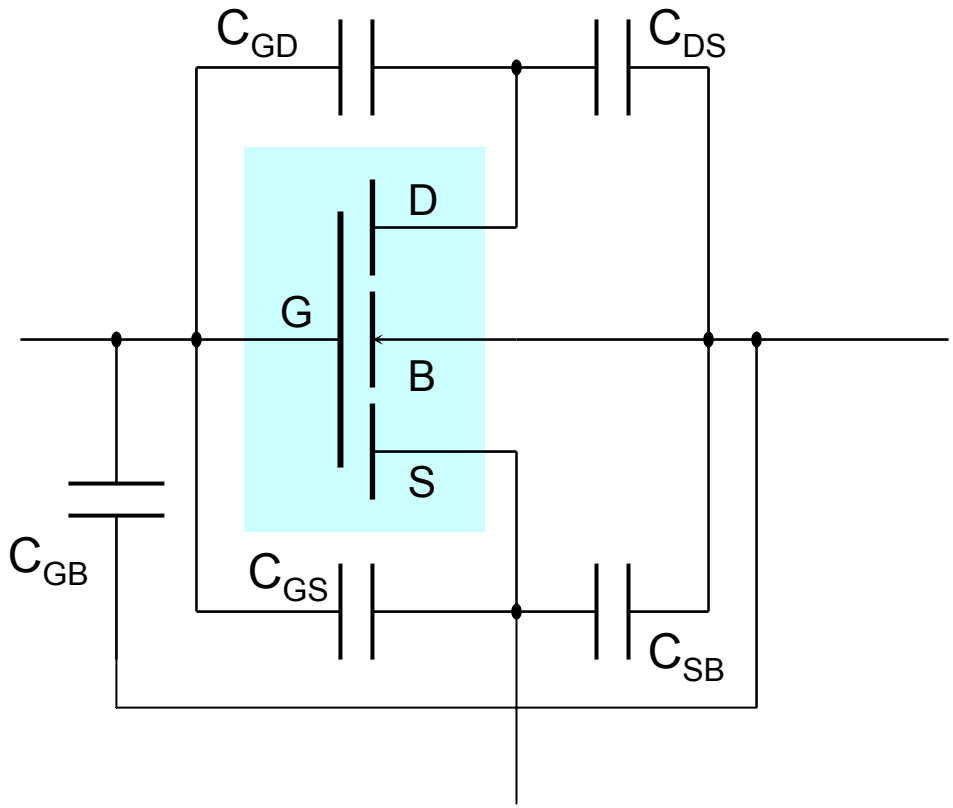


Long Channel

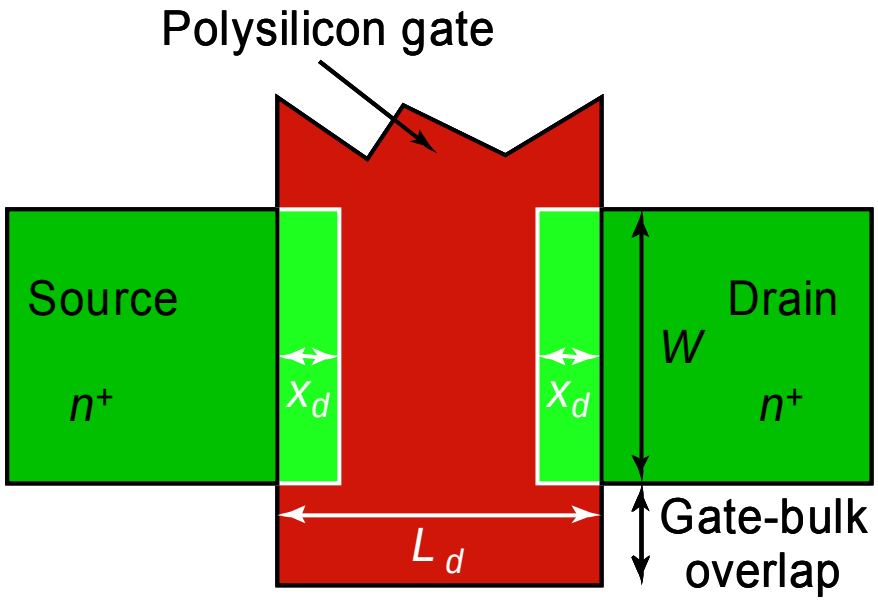


Short Channel

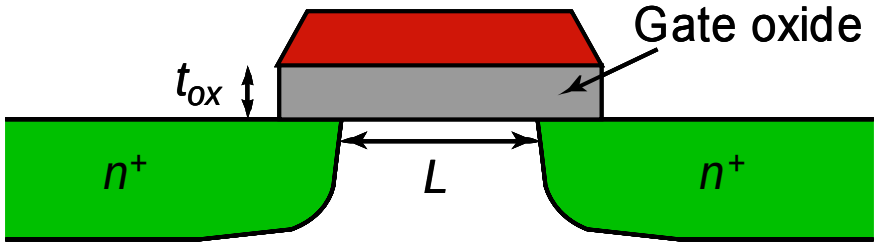
Dinamičko ponašanje MOS tranzistora
KAPACITIVNOSTI NMOS TRANZISTORA



KAPACITIVNOST GEJTA MOS TRANZISTORA



Top view

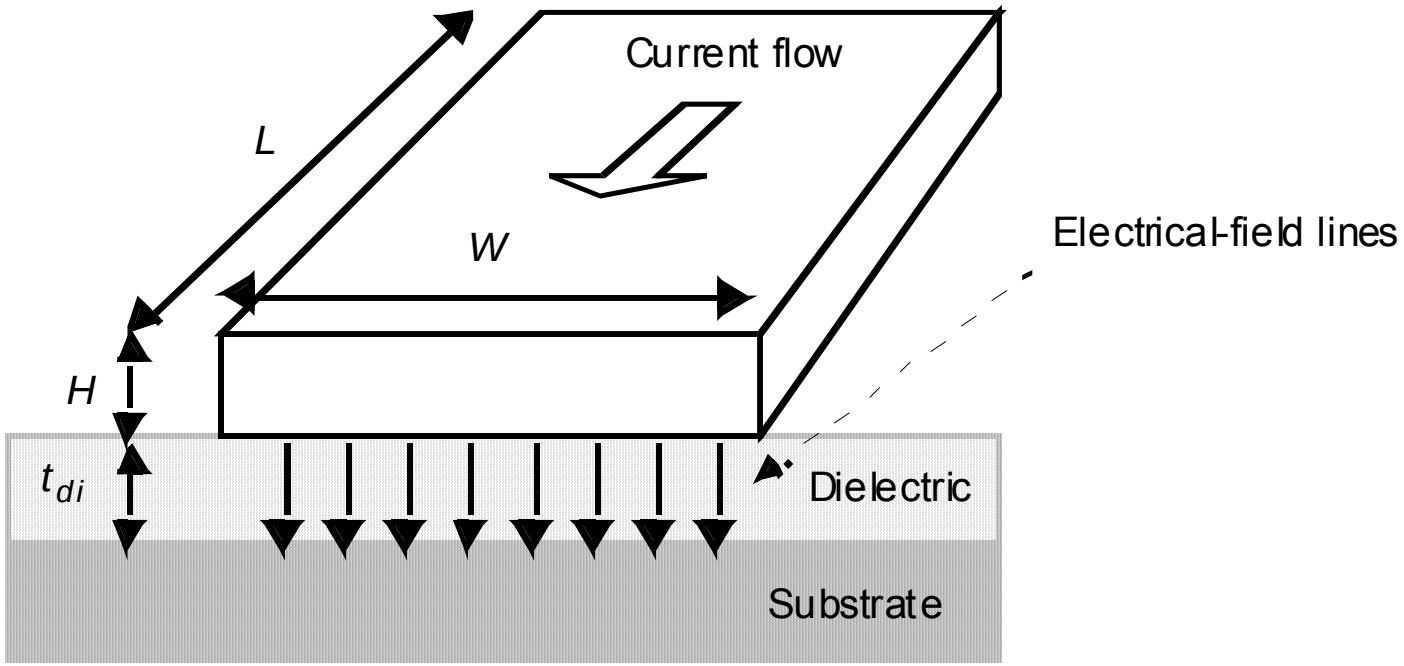


Cross section

$$C_{gate} = C_{gs} + C_{gd} + C_{gb}$$

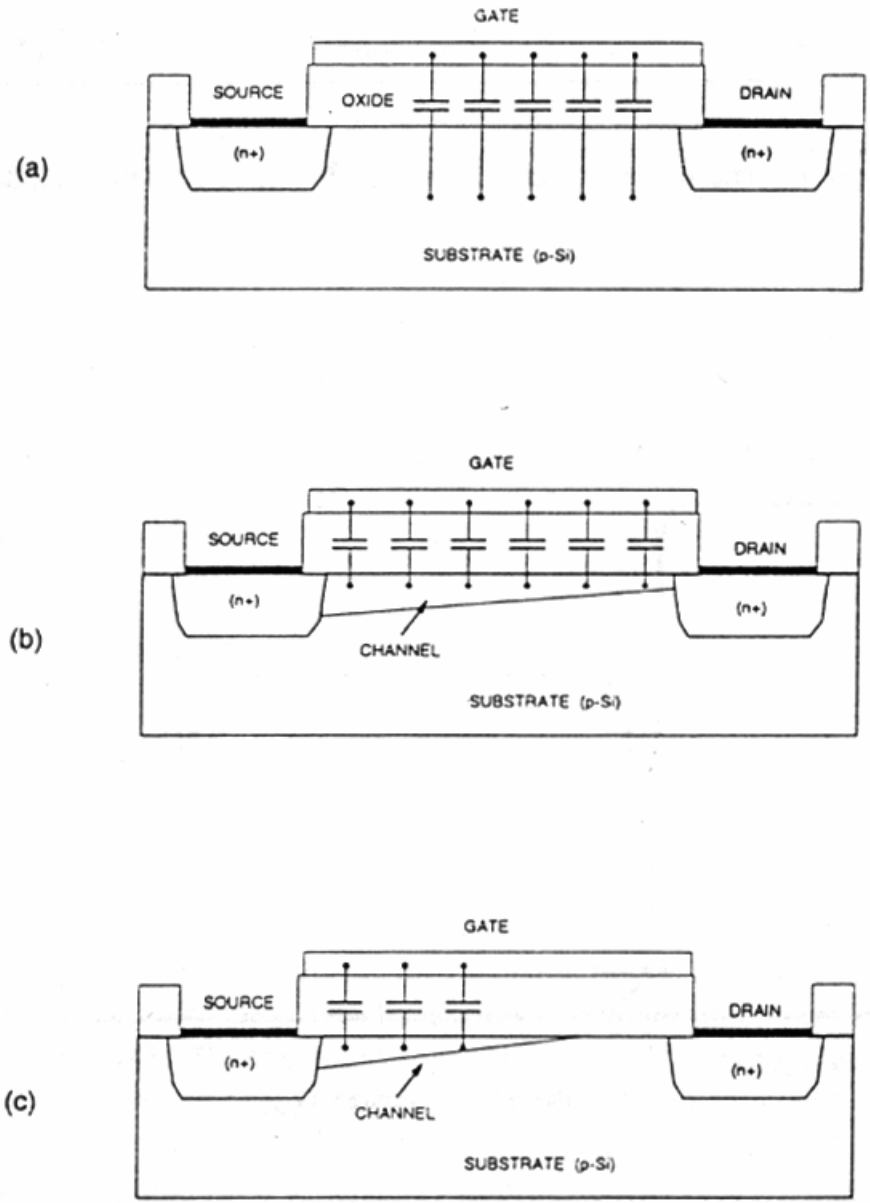
$$C_{gate} = \frac{\varepsilon_{ox}}{t_{ox}} WL$$

Capacitance: The Parallel Plate Model



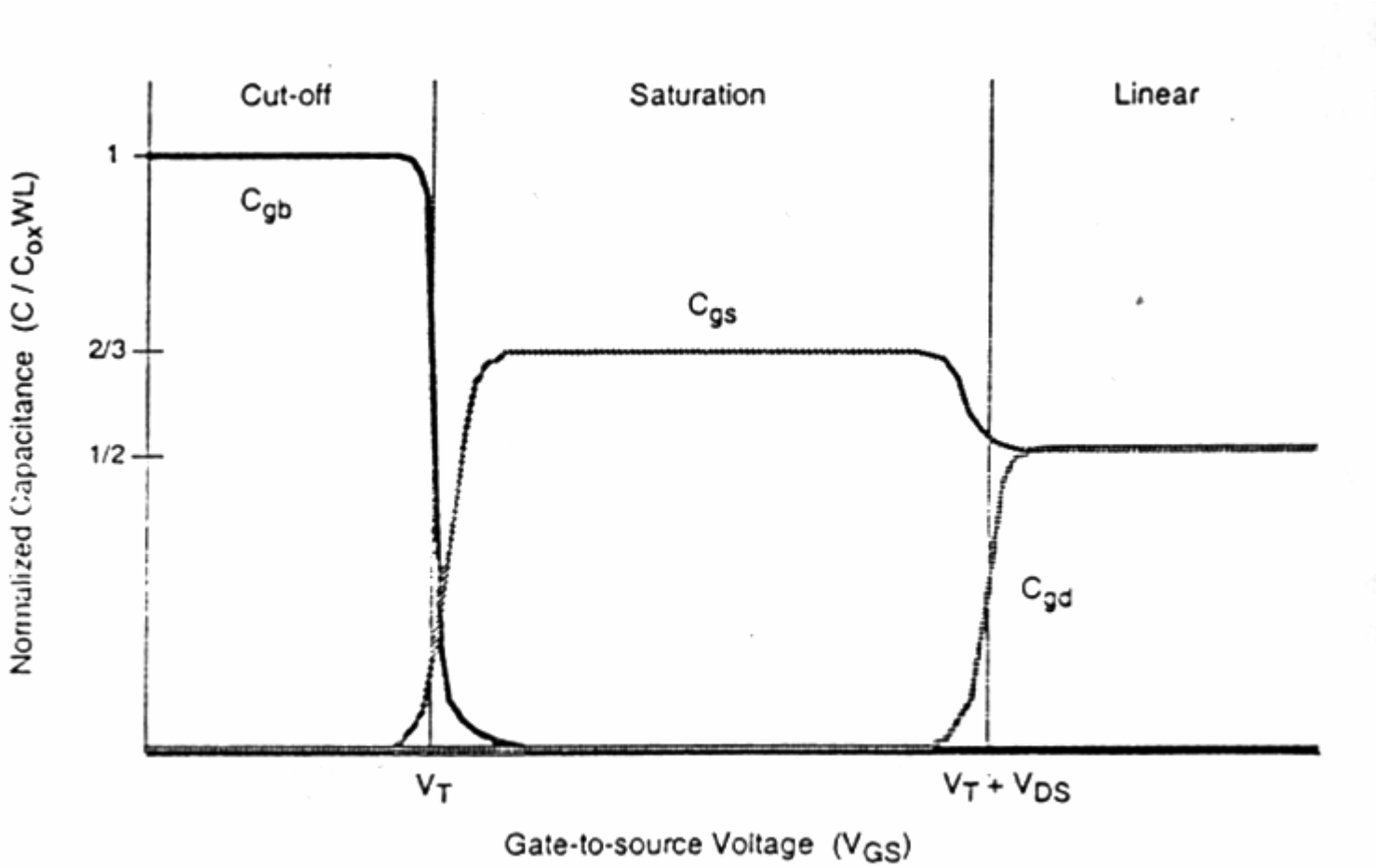
$$c_{int} = \frac{\varepsilon_{di}}{t_{di}} WL$$

$$S_{Cwire} = \frac{S}{S \cdot S_L} = \frac{1}{S_L}$$

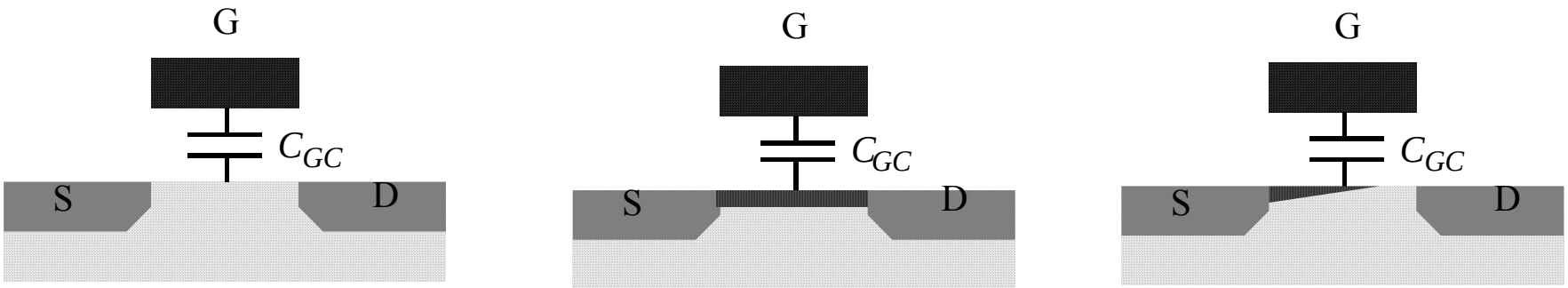


Kapacitivnost gejta pri zakocenju (a), linearnom rezimu (b) i zasicenju (c) MOS T-a

Varijacije kapacitivnosti gejta sa promenom Ugs



Gate Capacitance

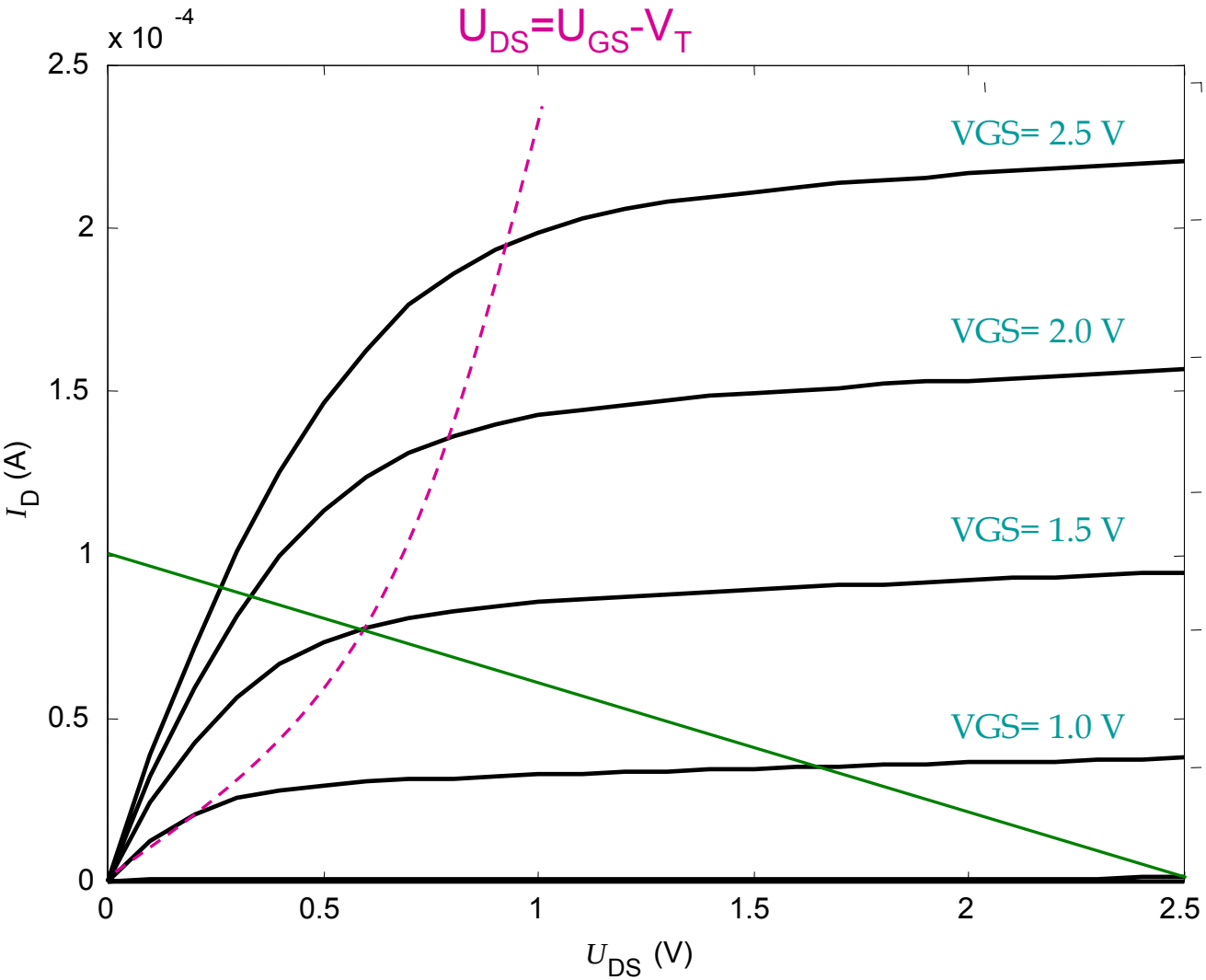


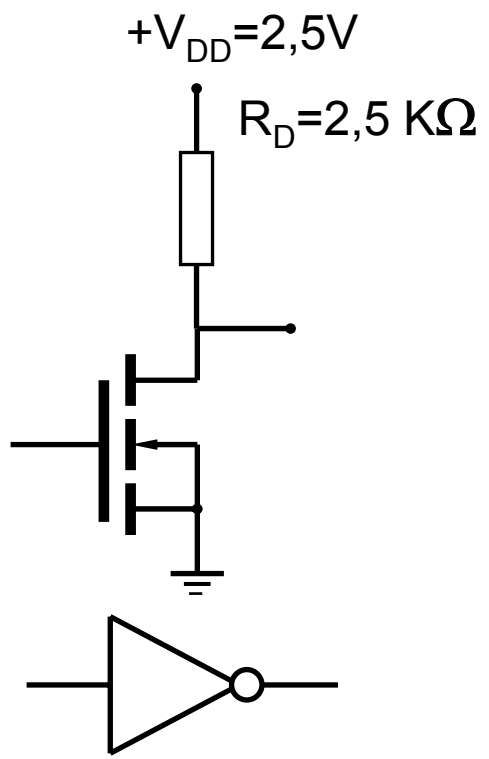
Operation Region	C_{gb}	C_{gs}	C_{gd}
Cutoff	$C_{ox}WL_{eff}$	0	0
Triode	0	$C_{ox}WL_{eff}/2$	$C_{ox}WL_{eff}/2$
Saturation	0	$(2/3)C_{ox}WL_{eff}$	0

Most important regions in digital design: saturation and cut-off

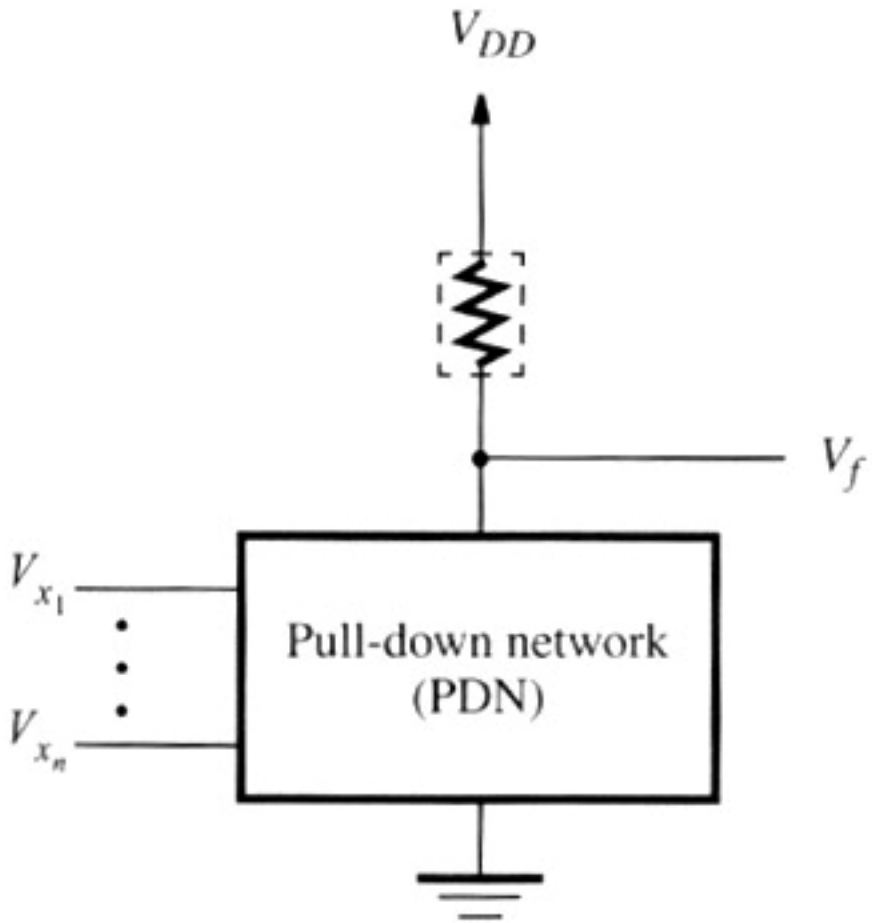
MOS FET KAO INVERTOR

$$I_D = k_n' \frac{W}{L}\left[(U_{GS} - V_T)V_{DS} - \frac{1}{2}U_{DS}^2\right] \qquad I_D = \frac{1}{2}k_n' \frac{W}{L}(U_{GS} - V_T)^2$$

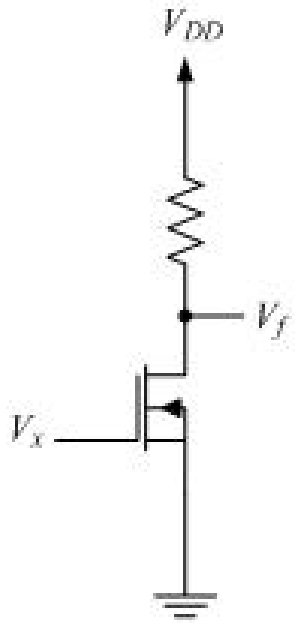




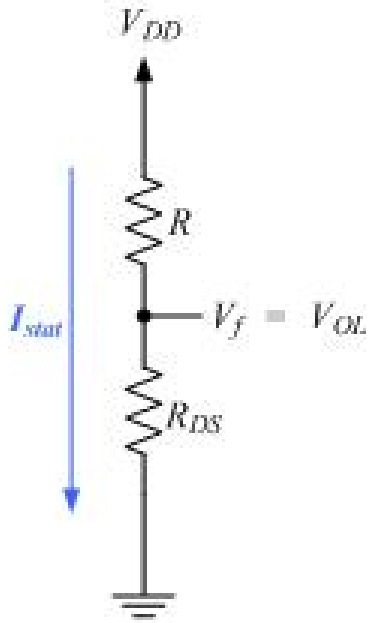
Struktura NMOS logičkih kola



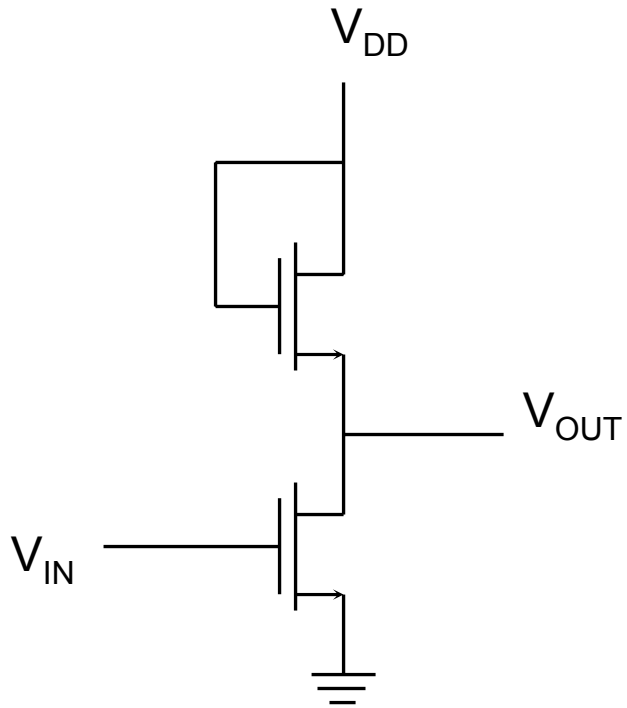
N-MOS INVERTOR



(a) NMOS invertor



(b) $V_x = 5$ V



$V(1)_{OUT} = V_{DD} - V_T$

Struktura CMOS logičkih kola